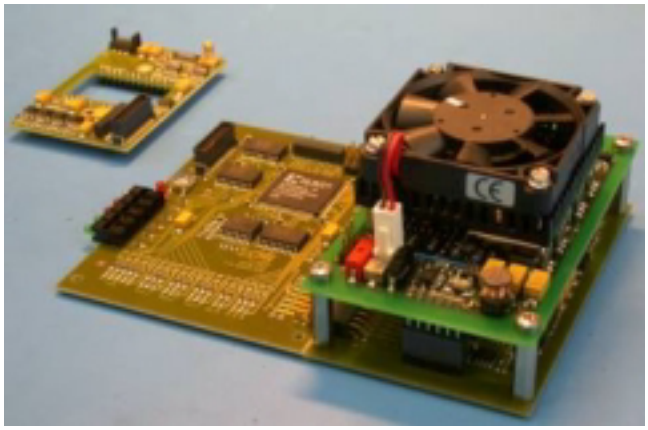
Preamplifier Electronics for CCD Arrays in UV/VIS Spectroscopy

The preamplifier electronics interfaces directly to the CCD chip. It provides all required digital signals for managing the readout process of the array. In addition it generates all necessary supply voltages from a single 12V DC input.

The preamplifier electronics connects to an Operating Electronics (Front End Electronics and Interface Electronics), where further data processing like AD conversion, buffering and data transfer to the computer is performed.



DZA-S703x electronics boards, shown with optional cooling controller

For Hamamatsu CCD series S703x and S701x

16 Bit Resolution

Various binning modes supported

Easy to integrate and use

Optional Cooling Controller available

Compatible to tec5 Operating Electronics

Supported Sensors / Detector Arrays

Supported CCDs:

Hamamatsu back thinned / back illuminated FFT-CCDs series S-7030, S-7033and S-7170 (uncooled) and S-7031, S7034 and S-7171 (one stage TE-cooled)
Hamamatsu front-illuminated FFT-CCDs series S-7010 (uncooled) and S-7011 (one stage TE-cooled)

Advantages for Applications

The series S703x of Hamamatsu back thinned/ back illuminated CCD arrays combines a high sensitivity over the whole spectral range from deep UV to NIR with the high dynamic range of a classical photodiode detector array. The series S701x from Hamamatsu are more cost-efficient front-illuminated types for applications not requiring UV-sensitivity. Both series are available with up to 1044 columns. Using these devices, all types of UV-VIS-NIR spectroscopy can be covered. The CCD's are especially suitable for low light level detection like fluorescence or diffuse reflection measurements. Due to the capability to detect even smallest amounts of light, short exposure times can be achieved in applications like high speed process control.

The preamplifier electronics provides an easy integration into the existing tec5 family of detector array Operating Electronics. This gives the user the benefit to extend the own product line by a CCD based device.
An optional temperature control board is available for the cooled CCD types.

Operation Modes

The preamplifier electronics supports a variety of binning modes, including line-binning, as well as the area readout mode.

Mode 'Line-binning'

In this operating mode, the information of all pixels in a column is combined. It imitates a classical 1D array for spectroscopy with a large pixel height, providing all the advantages of a large pixel area. The array data is compressed to a one dimensional format so that fast readout is possible due to the lower number of pixels.

Mode 'Imaging'

The imaging mode allows to access the information from each individual pixel. Various partial binning modes are possible.

Notice: Currently, the imaging mode is not supported by the subsequent Operating Electronics. Suitable electronics is in preparation.

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Board Arrangement

The preamplifier electronics is of modular design and, therefore, consists of several boards or functional units, respectively.

Sensor board:
small board for carrying the sensor chip. It has a big opening for access to the chip backplane. This allows to attach heat conducting devices for proper temperature control to the TE-cooled CCD types. The compact size allows easy integration in all optical setups, e.g. the distance of the chip to a spectrometer input can be very short, which ends up in a small split-off angle between optical input and output of the imaging spectrometer device.

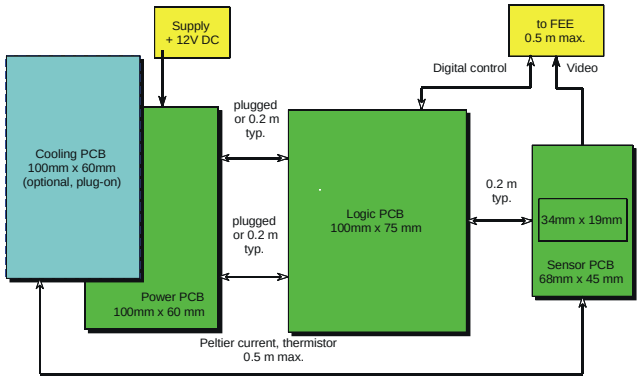
Logic board:
provides digital management of the sensor array (clocking and control / status functions)

Power supply board:
generates all necessary supply voltages for the unit out of +12 VDC.

Cooling controller board:
contains the temperature controller electronics to stabilize a set temperature of the sensor chip. The optional board can be slipped on to the power supply board.

All boards are interconnected by flat-ribbon cables.

For operation, a tec5 Operating Electronics with a Front End Electronics of type FEE-CCD is required.



Configuration of the CCD preamplifier electronics

Technical Data / Performance

Configuration:
line-binning mode

- readout time of a detector array with 1044 columns: less than 10 ms
- minimum integration time equivalent to readout time
- intensity resolution: 16 Bit
- dynamics: up to 15 bits with CCD
- operating mode selection by software via I2C or solder gaps
- modular board configuration
- supply: + 12 VDC, up to 3A (with temperature controller, depending on CCD type)

Products

■ **DZA-S7030-4-SLP**	**P/O 11-0101230-00**
■ **DZA-S7030-4-SLPC**	**P/O 11-0101233-00**
■ **DZA-S7010-1-SLP**	**P/O 11-0101234-00**
■ **DZA-S7010-1-SLPC**	**P/O 11-0101235-00**
■ **FEE-CCD**	**P/O 11-0106104-00**
■ **BE-PCI CCD/DZA**	**P/O 11-0101100-00**

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